FPGA-based Distributed Edge Training of SVM

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Motivation

- Training non-linear Support Vector Machine model
  *Computationally Expensive + Requires High Memory*

- FPGA-based SVM training accelerators exist, but, for
  *Sequential algorithms like SMO using single FPGA*

- Data is generally *Generated in a distributed* manner at edge

Contribution

*Train SVM model in a Distributed manner using Multiple FPGA network* while achieving

- Faster training time
- Memory-efficient data representations
- Negligible network communication overhead
- Linear Scalability with #FPGA units
- High Energy efficiency

Algorithmic Design

SVM learning

Process Flow for Distributed SVM algorithm (QRSVM)

A single QRSVM IP for FPGA

Multiple FPGA Network

Proof-of-Concept

Amazon AWS F1 instance with \( p=\{1,2,4,8\} \)

16nm Xilinx Virtex Ultrascale+ VU9P FPGA units