Laboratory Exercise #2
Inverter Characteristics and the Ring Oscillator

ECEN 248: Introduction to Digital Design

Department of Electrical and Computer Engineering
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1 Introduction

The purpose of this experiment is to introduce you to the concepts of Inverter voltage transfer characteristics, switching voltages, clocks, and gate delays. In this lab, we will first study the behaviour of a single inverter. Then we will cascade an odd number of inverters in a ring to create a *ring oscillator*.

2 Background

2.1 Voltage Transfer Characteristics

The voltage transfer characteristic of a device is a plot showing how the output voltage of a device varies with change in the input voltage. It is obtained by continuously varying the input voltage on the x-axis (independent) and output voltage on the y-axis (dependant). It is generally used to study the operation of a device. For example in Figure 1, the VTC can be used to determine that when the input voltage is 1V, then the output voltage is 5V.

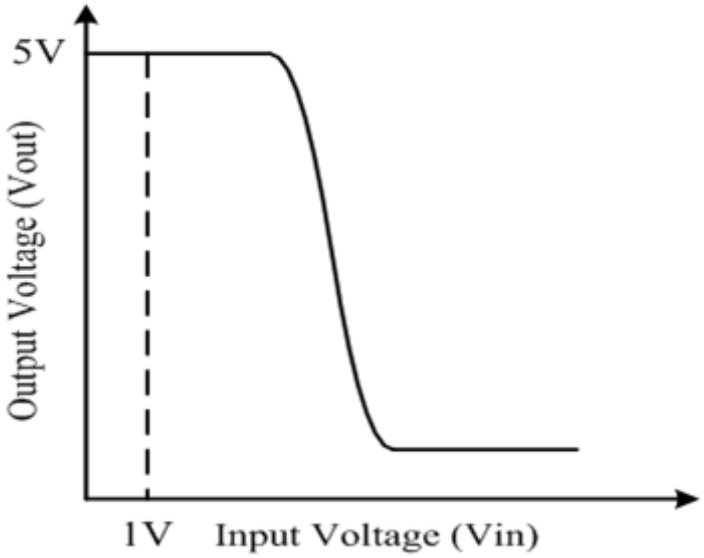

Figure 1: Voltage Transfer Characteristic

2.2 Ring Oscillator

A ring oscillator is a circuit composed of an odd number of inverter gates connected in a ring as shown in Figure 2. The NOT gates, or inverters, are arranged in a ring; the output of the last inverter is fed back into the first. Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation.

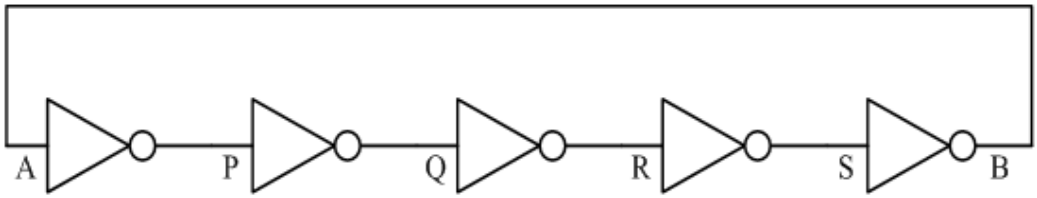

Figure 2: 5 Stage Ring Oscillator Circuit

In Figure 2, if the input value at *A* is 1 at time Φ and the delay of an inverter is *Dinv*, then the time at which a 0 will be fed back into the same node *A* is $\Phi + N * Dinv$ such that N is the number of inverters in the ring. Similarly, node A will be at logic level 1 again after a further delay $N * Dinv$. Therefore, the time period (T) of the ring oscillator is $2 * N * Dinv$, where N is the number of inverter stages in the ring oscillator and must be an odd number. The frequency of oscillation is $1/T$. The ring oscillator is an important circuit since it can be used to find the delay of a single inverter by measuring the time period of oscillation and dividing it by $2 * N$. This is helpful if $Dinv$ is too small to measure using the available equipment. Likewise, the ring oscillator can be used to generate a clock signal as shown in Figure 5.

3 Pre-lab

The TA will demonstrate the use of oscilloscope channel selection and automatic triggering, which is necessary to observe waveforms. No formal Pre-lab submission is required for this lab assignment.

4 Lab Procedure

Complete Experiments 1-2 listed below.

4.1 Experiment 1

In a circuit, logic values (i.e. 0 or 1) can be represented as levels of voltage. The most obvious way of representing two logic values as voltage levels is to define switching voltage levels.

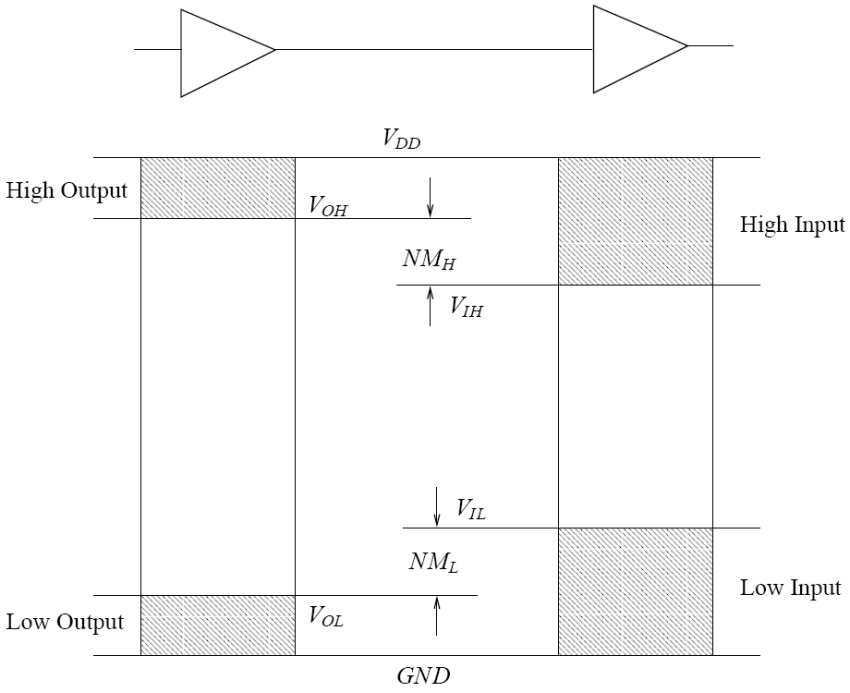

Figure 3: Voltage Switch Levels

To implement the switching voltage concept, a range of low and high voltage levels is defined, as shown in Figure 3 for input as well as output of an inverter. This figure indicates that voltages in the range Ground to VOL represent logic value 0 for the output of an inverter. Similarly, the range from V_{OH} to V_{DD} corresponds to logic value 1 of the output stage of the inverter. For the input of an inverter, the voltage range from Ground to V_{IL} represents logic value 0 and voltage range from V_{IH} to V_{DD} represent logic value 1. Logic signals do not normally assume voltages in undefined range except in transition from one logic value to the other. These voltage points are shown on the inverter VTC in Figure 4. For an inverter, NM_H and NM_L are defined as the high side and low side noise margins. Noise margins provide a cushion for noise immunity. If the V_{DD} or Ground of the driver glitches relative to the driven gate, the noise margins can provide noise immunity up to a certain level. The magnitude of glitch protection provided for by a digital circuit is given by the Noise margins. In our case for this experiment, assume V_{OL} and V_{OH} are Ground and V_{DD}, respectively.
Use the continuous voltage output pin of your power supply and connect it to input of an inverter gate and

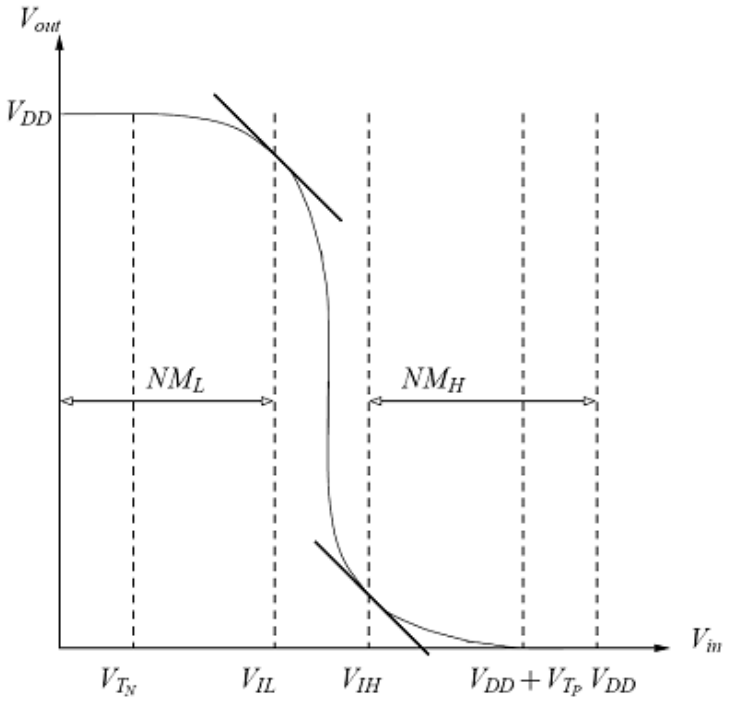

Figure 4: VTC of Inverter with Noise Margins

measure its output voltage with the multimeter while the input voltage of the gate sweeps from 0 to 5 volts. Draw the V_o vs. V_{in} curve for the inverter gate. Plot the VTC.

Note: Demonstrate the results to your TA.

4.2 Experiment 2

This experiment will introduce you concept of clock signals and circuit delays. A clock is a control signal that allows the changes in the states of digital circuits to occur only at welldefined time intervals. Since such a signal orchestrates the timing of a digital circuit, it is referred to as a clock. Typically, rising clock edges or falling clock edges lead to changes in the circuit states. Actually, a clock is a periodic signal with time period (T) (as shown in Figure 5) and a frequency $f = 1/T$.

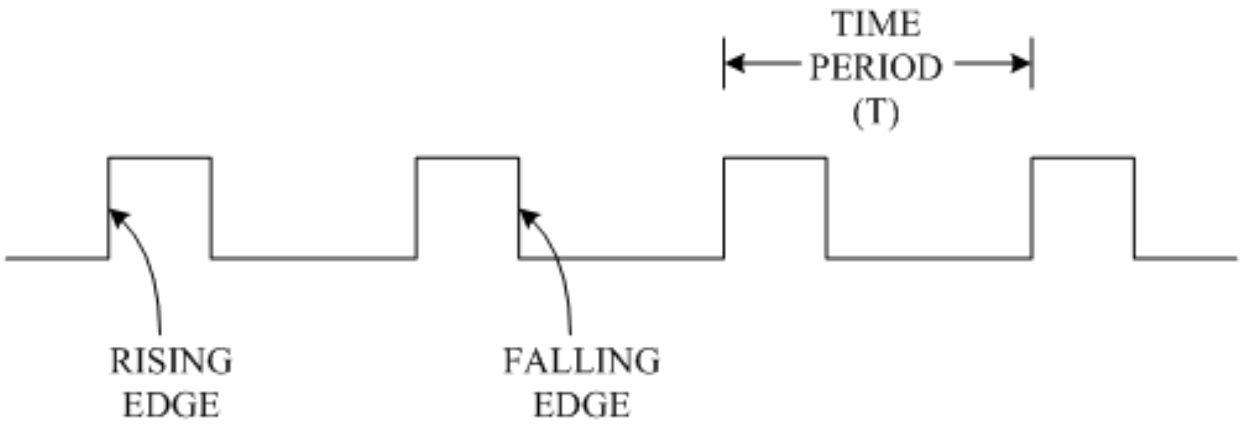

Figure 5: Sample Clock Signal

By connecting an odd number of inverter gates in a ring, you will create a circuit which generates a clock signal. Figure 2 depicts the simple a ring oscillator circuit such that $N = 5$. Connect the last gate output to first gate input. This feedback will cause the circuit to oscillate at a particular frequency. To see this signal on the oscilloscope, connect the output of any inverter to one of the oscilloscope channel and auto trigger that channel by pressing the "auto trigger" button on the front panel (below the LCD) of the oscilloscope. Then look at the output signal of any inverter in the ring on the oscilloscope and measure its time period and oscillation frequency. Then calculate average delay of a single gate.

Note: Demonstrate your results to the TA.

4.3 Post-Lab Deliverables

1. Plot the voltage transfer characteristics with V_{in} on x-axis and V_{out} on y-axis. Mark the range of voltages in output and input as Logic 0 and Logic 1. Determine the range of input voltage for which the inverter shows Logic 1 as output. Also determine the range of input voltage for which the inverter shows Logic 0 as output.

2. Derive the single-stage delay of the Ring Oscillator from the time period of oscillation that you see in Experiment 2. If the delay of one inverter is 10ns, what will be the frequency of the signal generated from a 21 stage ring oscillator?

3. Are the signals at P, Q, R, S in Figure 2 periodic? If so, what are their time periods? How do these signals differ from the signal at node A?

5 Important Student Feedback

The last part of lab requests your feedback. We are continually trying to improve the laboratory exercises to enhance your learning experience, and we are unable to do so without your feedback. Please include the following post-lab deliverables in your lab write-up.

Note: If you have any other comments regarding the lab that you wish to bring to your instructor's attention, please feel free to include them as well.

1. What did you like most about the lab assignment and why? What did you like least about it and why?

2. Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?

3. What suggestions do you have to improve the overall lab assignment?