Laboratory Exercise #4
Rudimentary Adder Circuits

ECEN 248: Introduction to Digital Design

Department of Electrical and Computer Engineering
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1   Introduction

The purpose of this laboratory assignment is to introduce you to the design of simple combinational adder circuits. In the pre-lab assignment, you will develop the designs for a half adder, full adder, and ripple carry adder. In the lab, you will bread-board and test your adder circuits. In addition to introducing you to simple arithmetic logic, this lab assignment will reinforce the use of Karnaugh Maps.

2   Background

In lab, we will be using two types of adder primitives, in particular half adders and full adders. These primitive components can be combined to create larger adders. The ripple carry adder is one such example. Each type of adder will be discussed below.

2.1   Half Adder Circuit

Figure 1 depicts a half adder circuit, which adds two input bits, A and B, together. Because each input bit can be 0 or 1, this adder computes a result between 0 and 2. The output bit, Sum (S), has the same significance as the inputs, A and B, while the carry-out bit (Cout) has twice the significance.
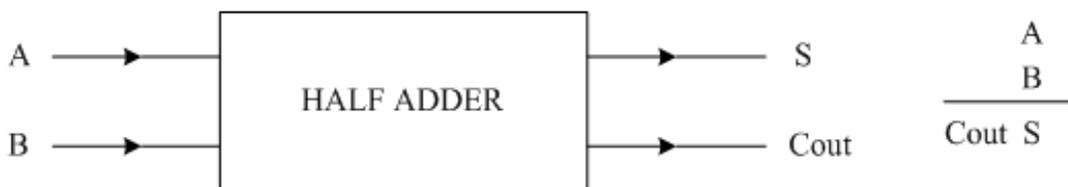

Figure 1: The Half Adder Circuit

2.2   Full Adder Circuit

A full adder circuit adds a carry-in bit (Cin) in addition to the two input bits, A and B, and produces a result between 0 and 3. See Figure 2. Like the half adder, the full adder has two output bits, S and Cout.
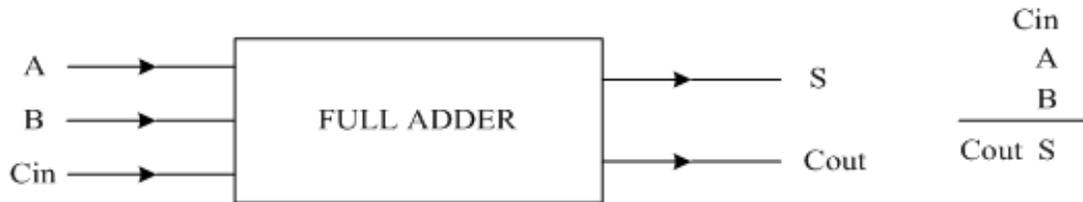
Figure 2: The Full Adder Circuit

2.3 The Ripple Carry Adder

The half and full adder circuits discussed above are useful primitives for performing addition on n-bit decimal numbers. The most elementary n-bit adder is the ripple carry adder showing in Figure 3. By feeding the carry-out bit of a full adder into the carry-in bit of another full adder, we can easily create a 2-bit ripple carry adder. We can continue to cascade n full adders in this manner to create an n-bit adder. This type of adder is appropriately named for the way the carries ripple across from the least significant to the most significant full adder. The correct result is not available until the ripple makes it to the last full adder, and it is for this reason that the ripple carry adder is only used for small values of n or in situations in which circuit delay is not an issue.
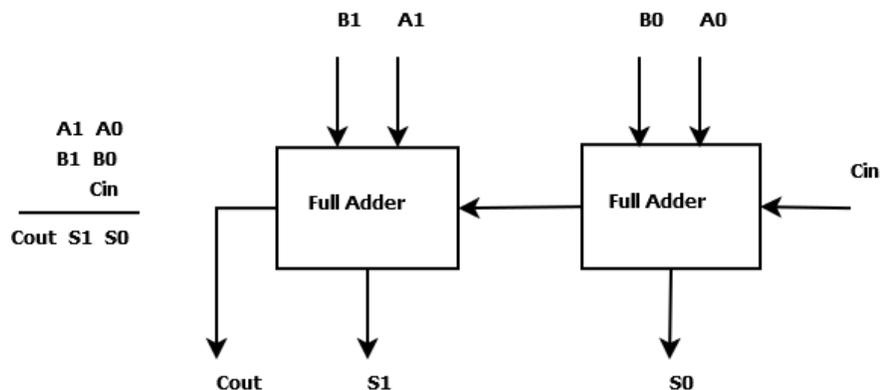

Figure 3: The Ripple Carry Adder Circuit

3 Pre-lab

3.1 Half Adder Design

Construct a truth table for a half adder circuit. From the truth table, create Karnaugh Maps for each output signal (i.e. S and Cout) and provide the minimized boolean algebra expressions for each output. Examine the truth table and boolean expression for an XOR gate (you should have create these for the previous post-lab write-up). If you were able to use XOR gates in addition to AND and OR gates in your half adder circuit, how many total gates would the half adder require? Is there an advantage to using XOR gates? Draw a gate-level schematic for the half-adder using a minimum number of gates. Assume you have XOR gates available for use.

3.2 Full Adder Design

Repeat the previous step for a full adder. Assume you can cascade XOR gates when more than 2 inputs are required.

3.3 Ripple Carry Adder Design

Design a 2-bit ripple carry adder using the full adder designed in the previous step. Consult Figure 3 for guidance. Your digital circuit should have two 2-bit inputs, {A1, A0} and {B1, B0}, and one single bit input, {Cin}. Similarly, it should have a 2-bit output, {S1 S0}, and a single bit output, {Cout}. Provide the truth table for the 2-bit adder. You do not have to compute the boolean expressions. Draw the gate-level schematic for the 2-bit ripple carry adder.

3.4 Pre-lab Deliverables

Please include the following items in your pre-lab write-up.

1. Truth table, K-maps, logic expressions without XORs, logic expressions with XORs, and gate-level schematic (reduced gate count) for Half Adder.

2. Truth table, K-maps, logic expressions without XORs, logic expressions with XORs, and gate-level schematic (reduced gate count) for Full Adder.

3. Truth table and gate-level schematic (reduced gate count) for 2-bit Ripple Carry Adder.

4 Lab Procedure

4.1 Experiment 1

Implement and test your half adder design using the gates in the Integrated Circuits (ICs) provided to you. Try to use the minimum number of gates (hint: use XORs where possible). Use the DIP switches to supply

input (A, B) into your circuit and display the output on two LEDs (Cout, S). Consult the previous lab if this is unclear.
Note: When your circuit is working, demonstrate your progress to the TA.

4.2 Experiment 2

Repeat Experiment 1 with your full adder design.
Note: When your circuit is working, demonstrate your progress to the TA.

4.3 Experiment 3

Implement and test your 2-bit ripple carry adder designed in the pre-lab. Use the DIP switches to provide the two 2-bit inputs and hardware the carry input to logic state 0. Display the result with the LEDs provided in your lab kit. Once working, test the circuit with a carry input of 1.
Note: Demonstrate the operation of your circuit to the TA with a carry input of 0 and 1.

5 Post-lab Deliverables

Please include the following items in your post-lab write-up in addition to the deliverables mentioned in the *Policies and Procedures* document.

1. Provide all design items found in the pre-lab deliverables. If you found that a design needed corrections while executing the lab, supply the updated version of that material.

2. Determine the worst case propagation delay for your full adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic. The maximum delay path is known as the critical path for that particular combinational block.

3. **(Honors)** Determine the worst case propagation delay for your 2-bit ripple carry adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic.

4. Design a 2-bit carry ripple adder assuming you only have half adder circuits and OR gates to work with. Draw up a schematic for your design using half adder building blocks and OR gates. Be sure the clearly label all inputs and outputs of your blocks.

5. **(Honors)** Determine the worst case propagation delay for your 2-bit ripple carry adder design using half adder circuits. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic.

6   Important Student Feedback

The last part of lab requests your feedback. We are continually trying to improve the laboratory exercises to enhance your learning experience, and we are unable to do so without your feedback. Please include the following post-lab deliverables in your lab write-up.

Note: If you have any other comments regarding the lab that you wish to bring to your instructor's attention, please feel free to include them as well.

1. What did you like most about the lab assignment and why? What did you like least about it and why?

2. Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?

3. What suggestions do you have to improve the overall lab assignment?