Appendix A

Integrated Circuit Pin Diagrams

- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

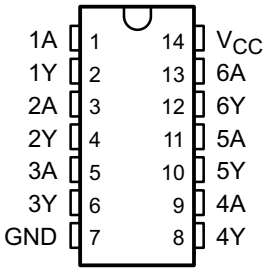
These devices contain six independent hex inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54ALS04B and SN54AS04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS04B and SN74AS04 are characterized for operation from 0°C to 70°C.

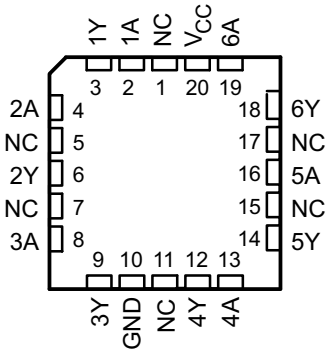
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

SN54ALS04B, SN54AS04 . . . J PACKAGE
SN74ALS04B, SN74AS04 . . . D OR N PACKAGE
(TOP VIEW)

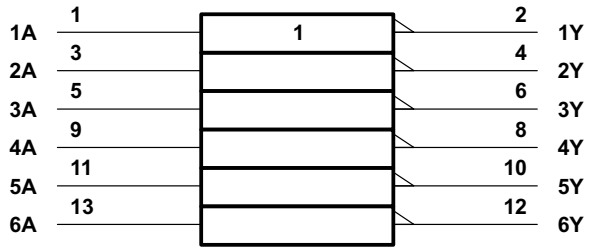


SN54ALS04B, SN54AS04 . . . FK PACKAGE
(TOP VIEW)



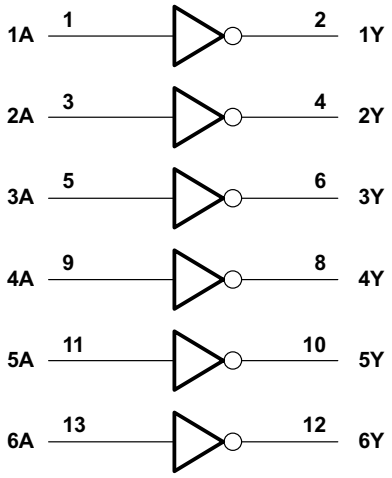
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

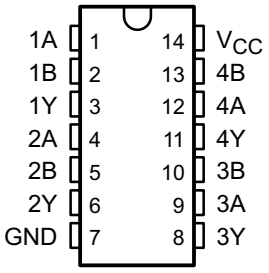
These devices contain four independent 2-input positive-AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

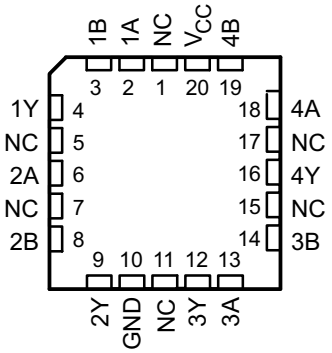
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SN54ALS08, SN54AS08 . . . J PACKAGE
SN74ALS08, SN74AS08 . . . D OR N PACKAGE
(TOP VIEW)

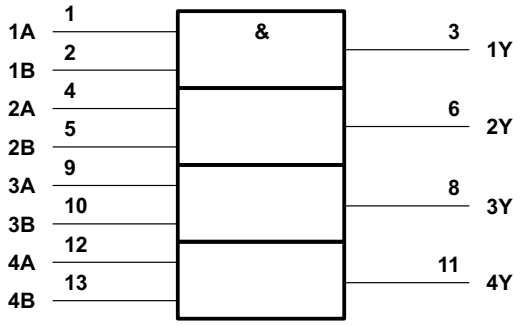


SN54ALS08, SN54AS08 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

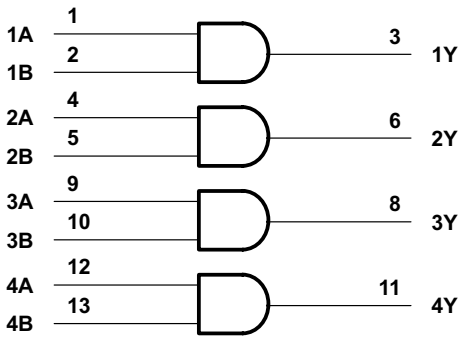
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

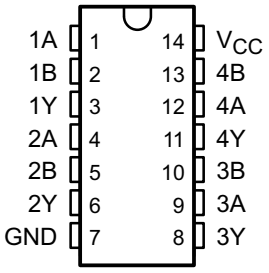
These devices contain four independent 2-input positive-OR gates. They perform the Boolean functions $Y = \overline{A} \bullet \overline{B}$ or $Y = A + B$ in positive logic.

The SN54ALS32 and SN54AS32 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS32 and SN74AS32 are characterized for operation from 0°C to 70°C.

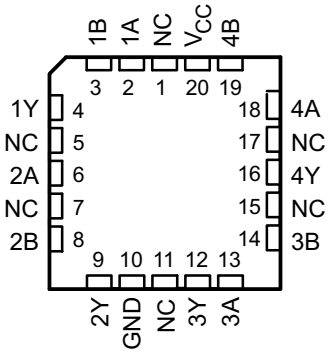
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54ALS32, SN54AS32 . . . J PACKAGE
SN74ALS32, SN74AS32 . . . D OR N PACKAGE
(TOP VIEW)

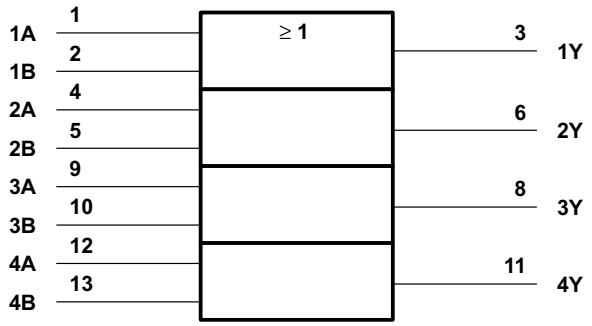


SN54ALS32, SN54AS32 . . . FK PACKAGE
(TOP VIEW)



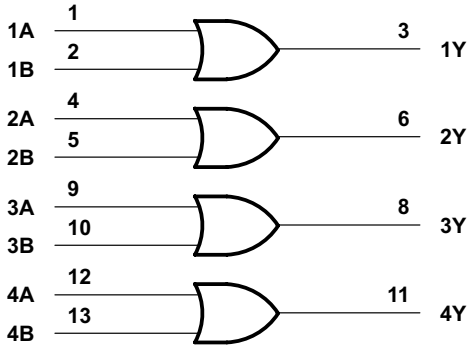
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

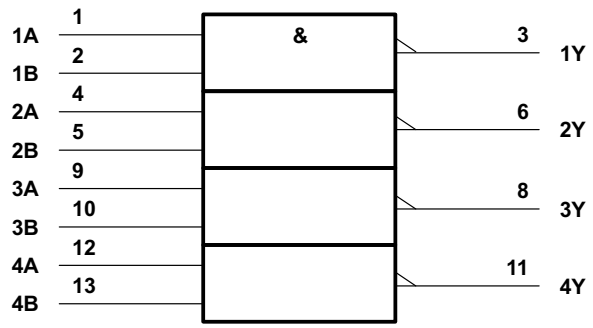
These devices contain four independent 2-input positive-NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS00A and SN54AS00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS00A and SN74AS00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each gate)

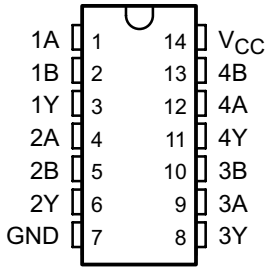
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

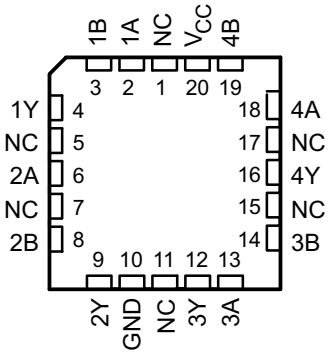


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

SN54ALS00A, SN54AS00 . . . J PACKAGE
SN74ALS00A, SN74AS00 . . . D OR N PACKAGE
(TOP VIEW)



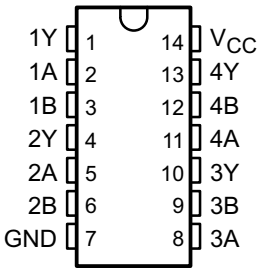
SN54ALS00A, SN54AS00 . . . FK PACKAGE
(TOP VIEW)



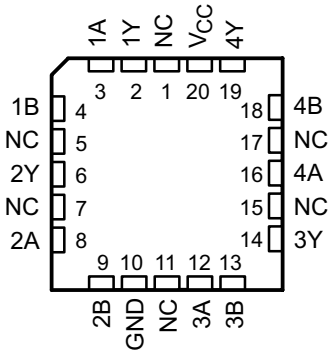
NC − No internal connection

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54AHCT02 . . . J OR W PACKAGE
SN74AHCT02 . . . D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \bullet \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54AHCT02 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHCT02 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	X	L
X	H	L
L	L	H

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

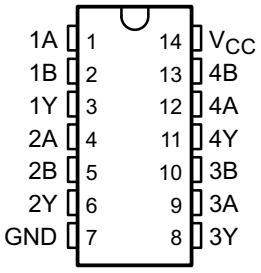
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54ALS86 and SN54AS86A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 and SN74AS86A are characterized for operation from 0°C to 70°C.

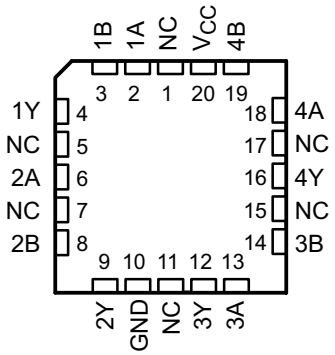
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SN54ALS86, SN54AS86A . . . J PACKAGE
SN74ALS86, SN74AS86A . . . D OR N PACKAGE
(TOP VIEW)

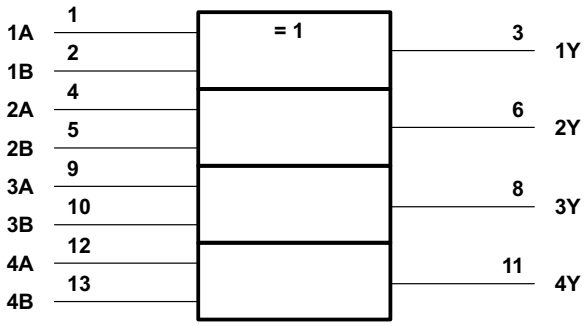


SN54ALS86, SN54AS86A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

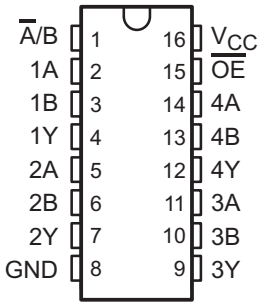
logic symbol†



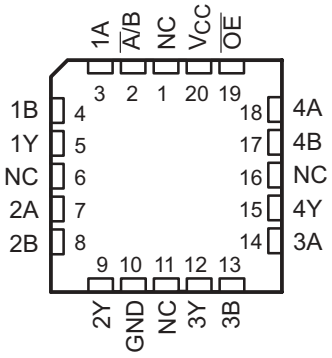
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

- **Operating Voltage Range of 4.5 V to 5.5 V**
- **High-Current 3-State Outputs Interface Directly With System Bus**
- **Typical t_{pd} = 17 ns**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **Provide Bus Interface From Multiple Sources in High-Performance Systems**
- **Buffered Inputs and Outputs**

SN54HCT257 . . . J PACKAGE
SN74HCT257 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT257 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ’HCT257 devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at the high logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

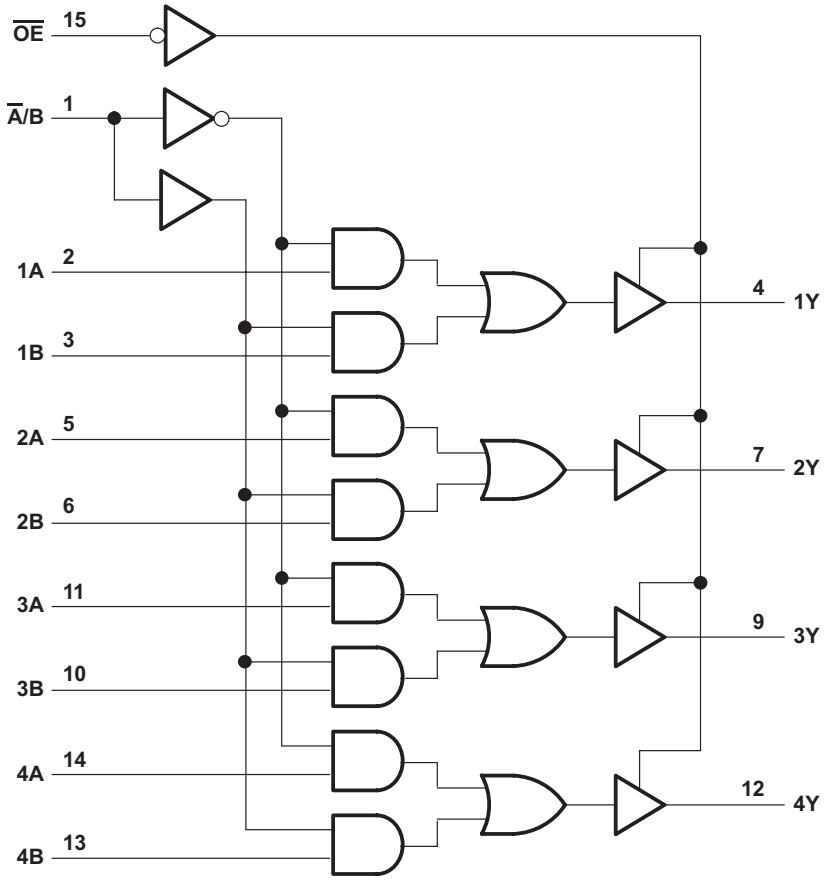
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HCT257N	SN74HCT257N
	SOIC − D	Tube of 40	SN74HCT257D	HCT257
		Reel of 2500	SN74HCT257DR	
		Reel of 250	SN74HCT257DT	
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54HCT257J	SNJ54HCT257J
	LCCC − FK	Tube of 55	SNJ54HCT257FK	SNJ54HCT257FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT Y
$\overline{OE}$	SELECT $\overline{A}$/B	DATA A	DATA B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

CD74HC283, CD74HCT283

High Speed CMOS Logic 4-Bit Binary Full Adder with Fast Carry

Data sheet acquired from Harris Semiconductor
SCHS176

November 1997

Features

- Adds Two Binary Numbers
- Full Internal Lookahead
- Fast Ripple Carry for Economical Expansion
- Operates with Both Positive and Negative Logic
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The Harris CD74HC283 and CD74HCT283 binary full adders that add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

Ordering Information

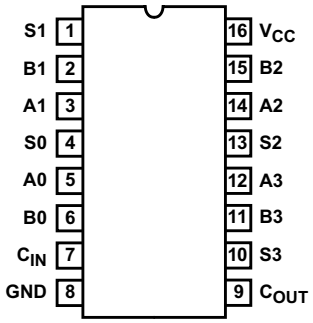
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC283E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT283E	-55 to 125	16 Ld PDIP	E16.3
CD74HC283M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT283M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

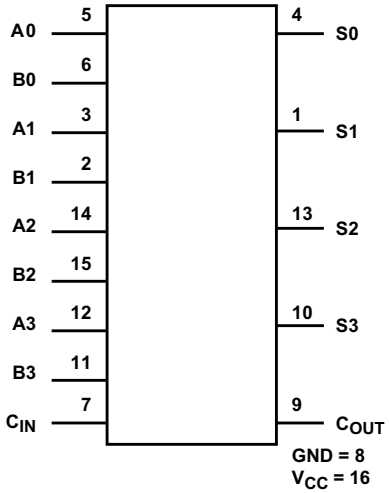
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout

CD74HC283, CD74HCT283
(PDIP, SOIC)
TOP VIEW



Functional Diagram



SN54246, SN54247, SN54LS247, SN54LS248
SN74246, SN74247, SN74LS247, SN74LS248
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

MARCH 1974—REVISED MARCH 1988

'246, '247, 'LS247 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

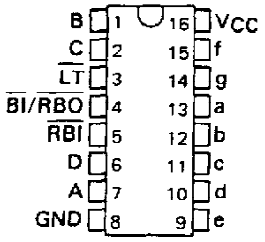
'LS248 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

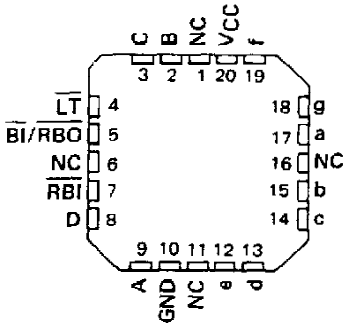
- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54246	low	open-collector	40 mA	30 V	320 mW	J,W
SN54247	low	open-collector	40 mA	15 V	320 mW	J,W
SN54LS247	low	open-collector	12 mA	15 V	35 mW	J,W
SN54LS248	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J,W
SN74246	low	open-collector	40 mA	30 V	320 mW	J,N
SN74247	low	open-collector	40 mA	15 V	320 mW	J,N
SN74LS247	low	open-collector	24 mA	15 V	35 mW	J,N
SN74LS248	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J,N

SN54246, SN54247 . . . J PACKAGE
SN54LS247 THRU SN54LS248 . . . J OR W PACKAGE
SN74246, SN74247 . . . N PACKAGE
SN74LS247, SN74LS248 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS247, SN54LS248 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

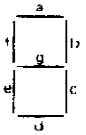
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

description

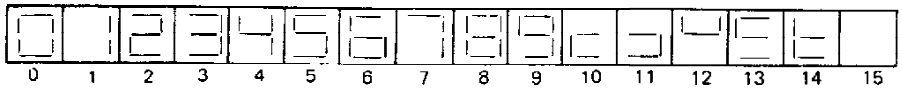
The '246 and '247 are electrically and functionally identical to the SN5446A/SN7446A, and SN5447A/SN7447A respectively, and have the same pin assignments as their equivalents. The 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '46A, '47A, 'LS47, and 'LS48 compose the 6 and the 9 without tails and the '246, '247, 'LS247, and 'LS248 compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the 'LS248 features active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.



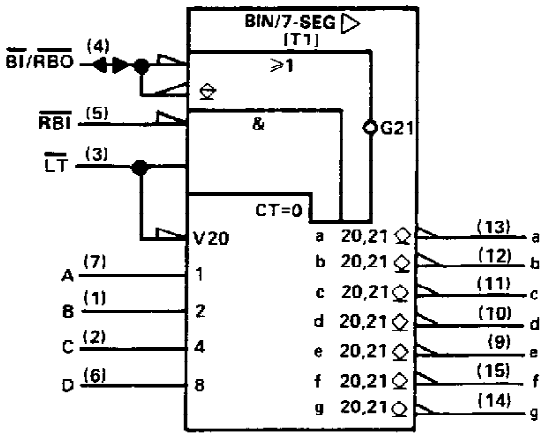
SEGMENT IDENTIFICATION



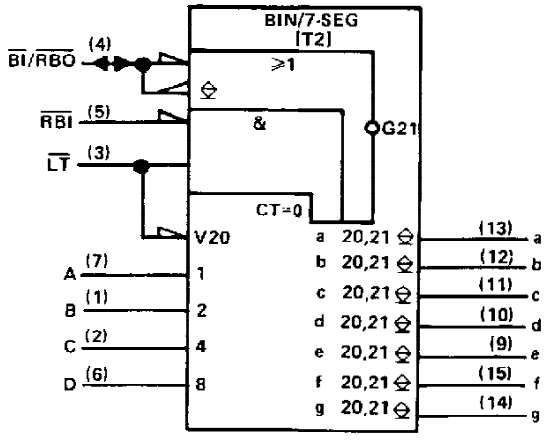
NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

logic symbols†

'246, '247, 'LS247



'LS248



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

'246, '247, 'LS247 FUNCTION TABLE (T1)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
$\overline{BI}$	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
$\overline{RBI}$	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
$\overline{LT}$	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

'LS248 FUNCTION TABLE (T2)

DECIMAL OR FUNCTION	INPUTS						$\overline{BI}/\overline{RBO}$†	OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	1
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

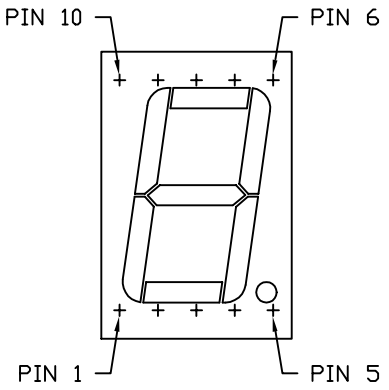
NOTES: 1. The blanking input ($\overline{BI}$) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output ($\overline{RBO}$) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

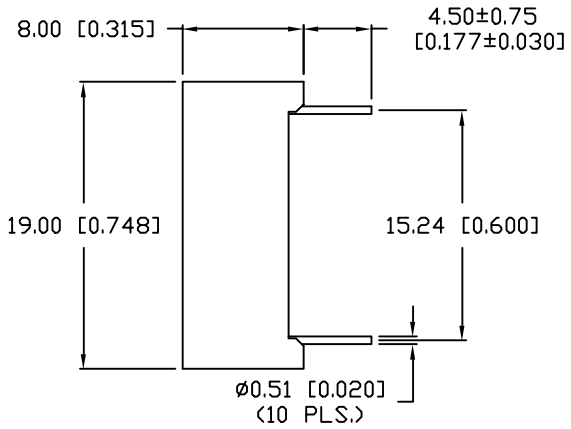
† $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$).

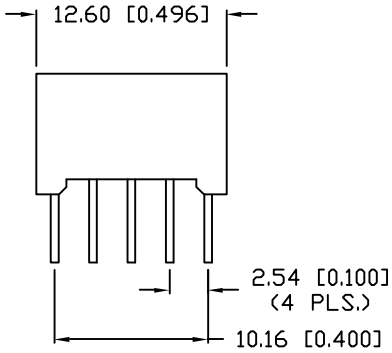
UNCONTROLLED DOCUMENT

PART NUMBER	REV.
LDS-A512RI	B

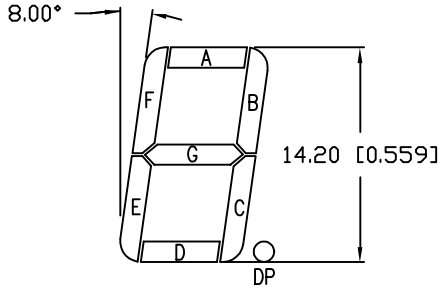
REV.	E.C.N. NUMBER AND REVISION COMMENTS	DATE
A	E.C.N. #10141.	4-8-96
B	E.C.N. #10BRDR. & REDRAWN.	5-11-99







CHARACTER DETAIL



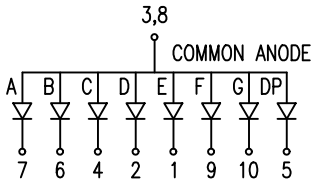
ELECTRO-OPTICAL CHARACTERISTICS T_A=25°C I_f=10mA

PARAMETER	MIN	TYP	MAX	UNITS	TEST COND
PEAK WAVELENGTH		565 (GREEN)		nm	
FORWARD VOLTAGE		2.2	2.6	V_f	
REVERSE VOLTAGE	5.0			V_r	I_r=100µA
AXIAL INTENSITY		3900		µcd	I_f=10mA
EMITTED COLOR:	GREEN				
FACE COLOR:	GRAY				
SEGMENT COLOR:	MILKY WHITE DIFFUSED				

LIMITS OF SAFE OPERATION AT 25°C PER CHIP

PARAMETER	MAX	UNITS
PEAK FORWARD CURRENT*	150	mA
STEADY CURRENT	25	mA
POWER DISSIPATION	105	mW
DERATE FROM 25°C	-1.2	mW/°C
OPERATING, STORAGE TEMP.	-40 TO +85	°C
SOLDERING TEMP.	+260	°C
2.0mm FROM BODY		3 SEC. MAX

* t<10µS



UNCONTROLLED DOCUMENT

*UNLESS OTHERWISE SPECIFIED TOLERANCE IS ±0.25mm (±0.010")

REV.	PART NUMBER
B	LDS-A512RI

0.56" SEVEN SEGMENT, SINGLE DIGIT DISPLAY,
565nm GREEN CHIPS, GRAY FACE WITH WHITE SEGMENTS,
COMMON ANODE, RIGHT DECIMAL.

RELIABILITY NOTE
OUR MANY YEARS OF EXPERIENCE DATA ACCUMULATION INDICATE THAT SOLDER HEAT IS A MAJOR CAUSE OF EARLY AND FUTURE FAILURE. PLEASE PAY ATTENTION TO YOUR SOLDERING PROCESS.

LUMEX INCORPORATED
290 E. HELLEN ROAD
PALATINE, ILLINOIS 60067
PHONE: 1-847-359-2790
WEB: HTTP://WWW.LUMEX.COM

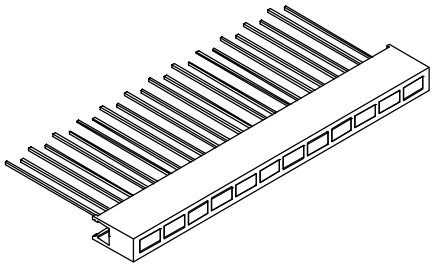
B

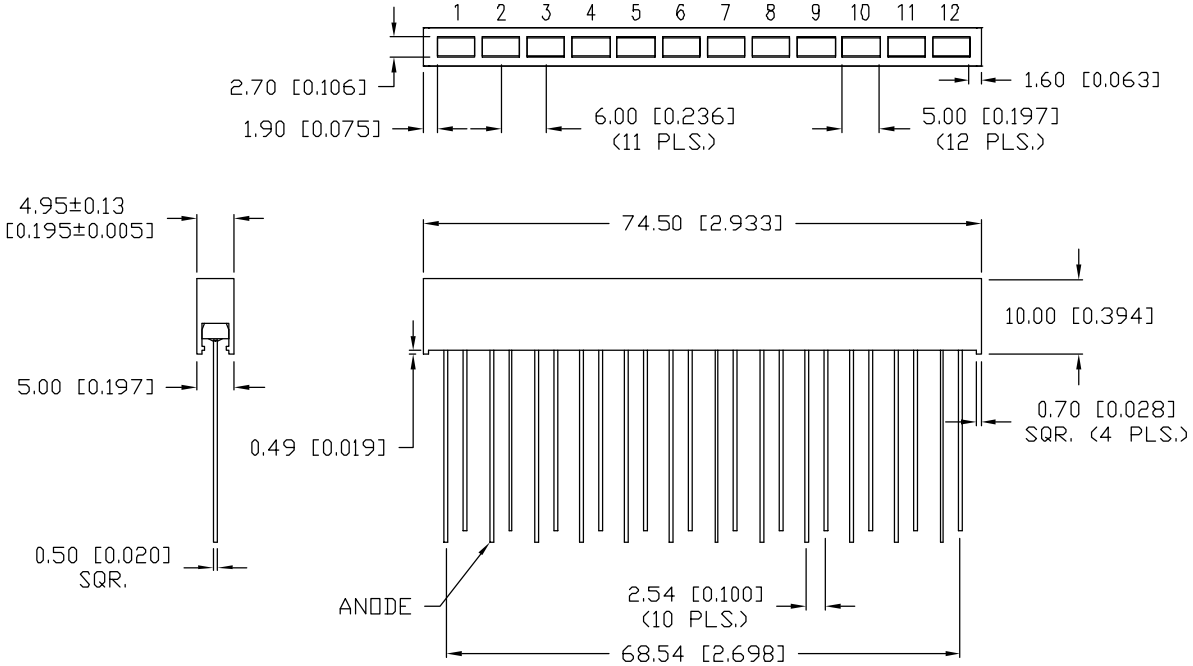
DRAWN BY:	CHECKED BY:	APPROVED BY:	DATE: 7-20-95
BC			PAGE: 1 OF 1
			SCALE: N/A

UNCONTROLLED DOCUMENT

PART NUMBER	REV.
SSA-LXH1225ID	A

REV.	E.C.N. NUMBER AND REVISION COMMENTS	DATE
A	E.C.N. #10BRDR. & REDRAWN.	6.8.01





ELECTRO-OPTICAL CHARACTERISTICS T_A=25°C I_f = 20mA

PARAMETER	MIN	TYP	MAX	UNITS	TEST COND
PEAK WAVELENGTH		635		nm	
FORWARD VOLTAGE		2.0	2.8	V_f	
REVERSE VOLTAGE	5.0			V_r	I_r=100µA
AXIAL INTENSITY		10		mcd	I_f = 20mA
VIEWING ANGLE		110		2x theta	
EMITTED COLOR:	RED				
EPOXY LENS FINISH:	RED DIFFUSED				

LIMITS OF SAFE OPERATION AT 25°C PER DIE

PARAMETER	MAX	UNITS
PEAK FORWARD CURRENT*	155	mA
STEADY CURRENT	30	mA
POWER DISSIPATION	110	mW
DERATE FROM 25°C	-1.2	mW/°C
OPERATING, STORAGE TEMP.	-40 TO +85	°C
SOLDERING TEMP.	+260	°C
2.0mm FROM BODY		3 SEC. MAX

* t<10µS

NOTES:

1. SSH-LXH1225 HOLDER, BLACK ABS UL 94V-0.
2. SSL-LX25583ID, LED. (12 PCS.)

UNCONTROLLED DOCUMENT

*UNLESS OTHERWISE SPECIFIED TOLERANCES PER DECIMAL PRECISION ARE: X=±1 (±0.039), X.X=±0.5 (±0.020), X.XX=±0.25 (±0.010), X.XXX=±0.127 (±0.005). LEAD SIZE=±0.05 (±0.002), LEAD LENGTH=±0.75 (±0.030). MIN= +DECIMAL PRECISION -0.00 MAX.= +0.00 -DECIMAL PRECISION

REV.	PART NUMBER
A	SSA-LXH1225ID

2.5mm x 5mm 12 LED RECTANGULAR ARRAY,
635nm HIGH INTENSITY RED LEDS, RED DIFFUSED.

RELIABILITY NOTE
OUR MANY YEARS OF EXPERIENCE DATA ACCUMULATION INDICATE THAT SOLDER HEAT IS A MAJOR CAUSE OF EARLY AND FUTURE FAILURE. PLEASE PAY ATTENTION TO YOUR SOLDERING PROCESS.

LUMEX INC. We Lume Photons To Work For You
290 E. HELEN ROAD
PALATINE, IL 60067-6976
PHONE: +1.847.359.2790
US WEB: www.lumex.com
TW WEB: www.lumex.com.tw

DRAWN BY:	CHECKED BY:	APPROVED BY:	DATE: 8.19.93
CT			PAGE: 1 OF 1
			SCALE: N/A

Appendix B

Generic User Constrained File for Xilinx Spartan 3E Starter Board

```
##############################################################
### SAMPLE SPARTAN-3E STARTER KIT BOARD CONSTRAINTS
##############################################################

# ==== Pushbuttons (BTN) ====
NET "BTN_EAST" LOC = "H13" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_NORTH" LOC = "V4" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_SOUTH" LOC = "K17" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "BTN_WEST" LOC = "D18" | IOSTANDARD = LVTTL | PULLDOWN ;

# ==== Clock inputs (CLK) ====
NET "CLK_50MHZ" LOC = "C9" | IOSTANDARD = LVCMOS33 ;

# ==== Character LCD (LCD) ====
NET "LCD_E" LOC = "M18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RS" LOC = "L18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RW" LOC = "L17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
# LCD data connections SF_D<3:0>
#NET "SF_D[0]" LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
#NET "SF_D[1]" LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
#NET "SF_D[2]" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
#NET "SF_D[3]" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# ==== Rotary Pushbutton Switch (ROT) ====
NET "ROT_A" LOC = "K18" | IOSTANDARD = LVTTL | PULLUP ;
NET "ROT_B" LOC = "G18" | IOSTANDARD = LVTTL | PULLUP ;
NET "ROT_CENTER" LOC = "V16" | IOSTANDARD = LVTTL | PULLDOWN ;

# ==== Discrete LEDs (LED) ====
NET "LED[0]" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[1]" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[2]" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[3]" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[4]" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[5]" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[6]" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "LED[7]" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# ==== ON/OFF Switches (SWITCH) ====
NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;
NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;
```