

## 1. Introduction

In Labs 1-8 you have implemented the design of a circuit using Custom Logic Design wherein the complete design process from the logic design to the layout of the gates and the placement of the gates in the final design is performed by you (the designer). Now, in Labs 9-12 we will see how this process can be automated by using a Hardware Description Language called Verilog, a synthesis tool called Design Analyzer and a Place and Route tool called Encounter.

## 2. General Design Flow

The design will begin in this lab with the description of a cruise control circuit for a vehicle using Verilog. In the following labs we will synthesize this circuit to generate the gate level description of the desired circuit. We then use the gate level netlist generated to place and route the circuit on which we will perform static timing analysis to see if the timing constraints on the circuit are satisfied.

## 3. Features of the Cruise Control Circuit

The cruise control circuit that you implement must include the following features:

- **Throttle:** This is the accelerator for the vehicle. This basically means that if this signal is on then the speed of the vehicle must increase every clock cycle.
- **Set:** This signal (pulse) is to set cruise control for the vehicle. If the speed of the vehicle is greater than 45mph then the cruise speed of the vehicle is locked to the speed of the vehicle at the instant when this signal was turned on. The vehicle will then travel at this cruise speed even if the throttle is turned off (i.e. we can take our foot of the accelerator of the vehicle). However even after **set** is activated, if the throttle is not turned off then the vehicle continues to accelerate according to the speed dictated by the throttle but if the throttle is turned off after some time, the vehicle has to slowly settle down at the speed set by the cruise control.

For example if the speed of the vehicle when **set** is applied is 50mph, then the cruise speed is set to 50mph, but if the throttle continues to be on then the speed at which the vehicle runs increases (every clock cycle) say till it reaches 60mph at which instant the throttle is turned off, then the speed of the vehicle will drop down to 50mph after which it continues to run at the cruise speed.

- **Accel:** This pulse has an effect only if the cruise control system of the vehicle has been set. Its effect is to increase the set cruise speed of the vehicle by 1mph.
- **Coast:** This pulse too has an effect only if the cruise control system of the vehicle has been set. Its effect is to decrease the set cruise speed of the vehicle by 1mph. Note: The cruise control should not work for a speed of less than 45mph.

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- **Cancel:** This pulse turns off the cruise control system of the vehicle.
- **Resume:** If the cruise control system of the vehicle had been turned off previously due to brake/cancel then the cruise control can be set again to the most recent speed that had been set.
- **Brake:** Pressing the brake will not only reduce the speed of the vehicle but will also turn **off** the cruise control system of the vehicle immediately.

You are required to implement the above features using Verilog. A behavioral description will be much easier to implement than a structural description of the circuit. The inputs to the circuits will be the above buttons and a clock signal to synchronize all operations but you may add a couple more signals for your convenience, but you will have to explain their utility in the report.

**NOTE: Not all verilog constructs are synthesizable (we eventually need to synthesize this logic in the next lab session). Hence take a look at the Pages 10 and 11 in “VerilogRef.pdf” which is put up on the website for all the supported constructs. For example, “initial” cannot be synthesized. Hence avoid using any non-synthesizable blocks in your design.**

### 4. Verification

You will also be required to write a test bench module using the above circuit to verify its operation in the following manner.

- Increase the speed of the vehicle to 30mph using **throttle**.
- Try to set cruise control using **set**. (It must fail).
- Continue to increase the speed to 50mph.
- Set the cruise speed at this point to 50mph.
- Continue to increase the speed (using throttle) of the vehicle to 60mph.
- Take the throttle off at this point. (The speed of the vehicle must then drop down to 50mph at every clock cycle after which the vehicle would cruise at the same speed).
- Now apply the brakes (i.e. provide a pulse at the **brake** input). This must turn the cruise control system off and the speed of the vehicle drops every clock cycle.
- When the speed of the vehicle is 30mph, provide a pulse at **resume**. The cruise control system is set again and the speed of the vehicle must then ramp up to 50mph.

### Simulation Details :-

You can use any verilog simulator of your preference. Cadence has its own verilog compiler and simulator called verilog XL. After creating the test bench and the design, you simulate it by entering the command

**verilog your\_tbench.v your\_module.v** where your\_tbench.v is the name of your test bench file and your\_module.v is the name of your verilog design file.

### 5. Report Requirements

1. Turn in the behavioral description of the code. Do use comments to explain the signals you have used in the code.
2. Provide inputs to the circuit such that the verification requirements as explained in the previous inputs are met. You will have to print out the following when you apply the inputs a) "speed" at which the vehicle is running. b) "cruise control" signal indicating if the cruise control system of the vehicle is on/off c) "cruise speed" of the vehicle (according to the requirements mentioned it is not necessary that the cruise speed of the vehicle be equal to its actual speed). Print out the outputs of the circuit and turn it in along with the code. It would also be easier if you could use the \$display statement to show what is happening in the test bench.