ECEN 350: Computer Architecture and Design

Spring 2015 (Credits: 4)
http://people.tamu.edu/~ehsanrohani/L350/index.htm

Instructor Information:
Name: Ehsan Rohani
Email address: ehsanrohani@tamu.edu
Office location: WERC 332A
Office hours: TRF (4p – 5p), By Appointment
Cell: (979)-422-7450
Site: http://people.tamu.edu/~ehsanrohani/

Course Description:
Computer architecture and design; use of register transfer languages and simulation tools to describe and simulate computer operation; central processing unit organization, microprogramming, input/output and memory system architectures. Cross-listed with CSCE 350.

Individual Course Objectives:
At the end of this course, students should:
✓ Understand the organization of a computer system including the CPU datapath, CPU control, and memory systems
✓ Understand the impact of semiconductor technology on computer design and architecture.
✓ Understand the basics and principles of instruction set design.
✓ Be familiar with programming using an assembly level language.
✓ Understand the impact of instruction sets on hardware design.
✓ Understand the basics of computer arithmetic, number representation, logic operations.
✓ Be familiar with designing datapaths for a processor.
✓ Understand the implications of branch instructions on program flow and hardware design.
✓ Understand the performance implications of various factors such as clock speed, average clock cycles per instruction and number of instructions.
✓ Understand the role of compilers and high-level languages in programming.
✓ Be familiar with designing control circuitry for a basic processor.
✓ Understand the differences in single-cycle/multicycle design of processors.
✓ Be familiar with processor pipelining.
✓ Understand the implications of pipelining on memory design, instruction set design, compiling, performance etc.
✓ Understand the implications of branch instructions on pipelining.
✓ Understand basics of memory technology, registers, SRAM, DRAM.
✓ Understand the performance issue of various memory technologies.
✓ Be familiar with the notion of locality.
✓ Understand the memory architectures including cache architectures.
✓ Be familiar with various cache architectures: direct-mapped, set-associative, wide/narrow block size etc.
✓ Understand the concepts of virtual memory.
✓ Be familiar with the need for address translation.
✓ Understand the impact of address translation on cache/memory accesses.
✓ Be familiar with hardware designs of various cache architectures.
✓ Understand the basics of Input/Output.
✓ Be familiar with magnetic disk drives and different components of accessing data from a disk drive.
✓ Be familiar with interrupt driven/ polling-driven I/O.
✓ Be familiar with basics of keyboard I/O, network I/O and graphics
✓ Understand register-transfer level (RTL) system concepts and description methods, including a hardware description language (VERILOG)

Prerequisite:
ECEN 248 – Introduction to Digital Systems Design.

Textbook and/or Resource Material:
Required:

Supplemental Texts:
“Starter’s Guide to Verilog 2001” by M. Ciletti, Prentice Hall; illustrated edition (September 29, 2003);
“A Verilog HDL Primer” by J. Bhasker, Star Galaxy Publishing; 3rd edition (January 2005);

Course Topics/Schedule:
Approximated Hours:  Topic
3 hours: Overview of Computer Architecture
3 hours: Instruction Set Architectures (ISA), Representing instructions on the computer, Arithmetical and logical instructions, Memory access instructions
3 hours: Instruction Set Architectures (ISA), Control flow instructions, Function calls instructions, Input-output instructions SPIM- instruction set simulator
3 hours: Computer Arithmetic, Signed and unsigned numbers, Addition and subtraction, Multiplication, Division, Floating point operations
3 hours: Translating and starting a program, Compilers, compiler optimization, Object code generation, assemblers, linking, Run-time execution environment
3 hours: Performance evaluation, CPU performance and its factors, performance metrics, performance factors, comparing performance, SPEC benchmarks
4 hours: Hardware Description Languages, Verilog hardware description language, Design-Simulation Process, Structural Designs in Verilog Behavioral HDL Description of Systems
3 hours: Datapath and Control, and ALU design
3 hours: Single-cycle implementation
3 hours: Microprogramming, catchup
3 hours: Pipelining, Pipelined datapath
4 hours: Pipelined control, Pipeline hazards: structural, control, data hazard detection and resolution, exception handling
4 hours: Memory Hierarchy, Overview of SRAM and DRAM design, Basic of caches, Framework for memory hierarchy, Measuring memory performance

**Grading Policies:**

**Breakdown:**

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<td>Exams</td>
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**Grading Scale:**

- A: 90-100%
- B: 80-89%
- C: 70-79%
- D: 60-69%
- F: 0-59%

(Note: in the event that the average overall grade of all students lies below a 79% there will be a curve on the overall grade. I will not curve the individual exams and assignments.)

**Exams:**

There will be one midterm and a final. The final will be cumulative, but with an emphasis on the material covered since the midterm. All tests are open-book, open notes.

**Tentative Test schedule:**

TBD
Assignments/Quizzes:
Rather than traditional homework, this course will rely upon a series of on-line quiz assessments. There will be approximately one quiz for each lecture. The goal of these quizzes will be to test your knowledge of the lecture material and pinpoint which lectures you should go back and review on-line. The TAMU eCampus system will be used for all quiz and Lab submissions. The two lowest quiz grades will be dropped.

Suggestions:
Suggestions for improvement are welcome at any time. Any concern about the course should be brought to the instructor’s attention.

Other Pertinent Course Information:
Excused absences:
Rules concerning excused absences may be found at http://student-rules.tamu.edu/rule07. In particular, except for absences due to religious obligations, the student must notify his or her instructor in writing (acknowledged e-mail message is acceptable) prior to the date of absence if such notification is feasible. In cases where advance notification is not feasible (e.g., accident, or emergency) the student must provide notification by the end of the second working day after the absence. This notification should include an explanation of why notice could not be sent prior to the class. If the absence is excused, the instructor must either provide the student with an opportunity to make up any quiz, exam or other graded activities or provide a satisfactory alternative to be completed within 30 calendar days from the last day of the absence.

Days of religious observance:
By state law, if a student misses class due to an obligation of his or her religion, the absence is excused.

Americans with Disabilities Act (ADA):
The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact Disability Services, in Cain Hall, Room B118, or call 845-1637. For additional information visit http://disability.tamu.edu

Academic Integrity:
“An Aggie does not lie, cheat, or steal, or tolerate those who do.”
Upon accepting admission to Texas A&M University, a student immediately assumes a commitment to uphold the Honor Code, to accept responsibility for learning and to follow the philosophy and rules of the Honor System. Students will be required to state their commitment on examinations, research
papers, and other academic work. Ignorance of the rules does not exclude any member of the Texas A&M University community from the requirements or the processes of the Honor System. For additional information please visit: http://aggiehonor.tamu.edu/ On all course work, assignments, and examinations at Texas A&M University, the following Honor Pledge shall be preprinted and signed by the student:

"On my honor, as an Aggie, I have neither given nor received unauthorized aid on this academic work."

Remember that plagiarism will not be tolerated and will be dealt with under the Aggie Honor System Office guidelines.